CLAIMS

What is claimed is:

1. A vertical Fin-FET semiconductor device characterized by:

at least one vertical semiconductor fin (12A) disposed on an insulator layer (4);

doped source (26A) and drain regions (28A) in bottom and top portions of the at least one semiconductor fin (12A); and

gate conductors (24A, 24B) disposed along vertical sidewalls of the at least one semiconductor fin (12A) and separated therefrom by thin gate insulators (22).

2. A vertical Fin-FET semiconductor device according to claim 1, further characterized by:

source conductors (18A, 18B) contacting the source region (26A) on opposite sides of the at least one semiconductor fin (12A);

at least one source contact (38A) connecting to at least one source conductor (18A, 18B);

at least one drain contact (40A) connecting to the drain region (28A) of the at least one semiconductor fin (12A);

a vertical channel region in the fin (12A) between the source region (26A) and the drain region (28A); and

at least one gate contact (42A) connecting to at least one gate conductor (24A, 24B).

3. A vertical Fin-FET device according to claim 2; wherein the at least one gate contact (42A) connects to two gate conductors (24A, 24B) on opposite sides of the same fin (12A).

4. A vertical Fin-FET device according to claim 2, further characterized by:

two gate contacts (42AA, 42BB), distinct from one another and each connecting to a respective gate conductor (24A, 24B) on opposite sides of the same fin (12A).

5. A vertical Fin-FET device according to claim 2, wherein the at least one drain contact (40A) connects to at least two source conductors (18A, 18B) on opposite sides of the same fin (12A).

6. A vertical Fin-FET device according to claim 2, wherein the gate conductors (24A, 24B) span a vertical distance between the source and drain regions (26A, 28A) in the at least one fin (12A).

7. A vertical Fin-FET device according to claim 2, further characterized by at least two vertical fins (112A, 112B Fig. 18).

8. A vertical Fin-FET device according to claim 2, wherein the at least one drain contact (40A, Fig. 15) laterally overextends the at least one fin (12A).

9. A vertical Fin-FET device according to claim 2, wherein:

the source conductors (18A, 18B) are n+ doped;

the gate conductors (24A, 24B) are n+ doped;

the source and drain regions (26A, 26B) are n+ doped; and

the channel is the fin (12A) p^- doped or intrinsic.

10. A vertical Fin-device according to claim 2, wherein:

the source conductors (18A, 18B) are p+ doped;

the gate conductors (24A, 24B) are p+ doped;

the source and drain regions (26A, 26B) are p+ doped;

the vertical Fin-FET device is an pFET device; and

the channel is the fin (12A) p^- doped or intrinsic.

11. A vertical Fin-FET device according to claim 1, wherein the insulator layer (4) is a buried oxide layer (BOX) of a SOI substrate.

12. A vertical Fin-FET device according to claim 2, wherein the vertical Fin-FET device is part of a CMOS circuit.

13. A vertical Fin-FET device according to claim 2, wherein the vertical Fin-FET device is part of an integrated circuit device.

14. A vertical Fin-FET device according to claim 2, wherein in the channel region, channels form adjacent to the gate insulators (22) and extending between the source region (26A) and drain region (28A) in response to a bias voltage applied to the gate conductors (24A, 24B)

15. A vertical Fin-FET device characterized by:

a thin vertical silicon fin (12A) formed in a silicon layer (6) of an SOI substrate;

doped source and drain regions (26A, 28A) formed in bottom and top portions, respectively, of the fin;

a pair of gate conductors (24A, 24B) disposed along opposite vertical sidewalls of the fin (12A), separated from the fin by thin gate insulators (22) and spanning a vertical distance between the source and drain regions (26A, 26B);

a pair of source conductors (18A, 18B) disposed alongside of and in contact with the source region (26A) on opposite sides of the fin (12A);

a drain contact (40A) connecting to the drain region (28A);

a source contact (38A) connecting to the source conductors (18A, 18B); and

at least one gate contact (42A) connecting to at least one gate conductor (24A).

16. A vertical Fin-FET device according to claim 14, wherein the at least one gate contact (42A) connects to both gate conductors (24A, 24B).

17. A vertical Fin-FET device according to claim 15, wherein:

the at least one gate contact (42AA) connects to one gate conductor (24A); and

a second gate contact (42AB) connects to another gate conductor (24B) on the opposite side of the same fin (12A).

18. A vertical Fin-FET device according to claim 15, wherein:

the drain contact (40A, Fig. 15) laterally overextends the fin 12A.

19. A vertical Fin-FET device according to claim 15, wherein:

the at least one gate contact (42A) connects to the at least one gate conductor (24A) via a respective silicide gate contact structure (32A, 32B); and

the source contact (38A), connects to the source conductors (18A, 18B) via silicide source contact structures 34A, 34B.

20. A method of forming a vertical Fin-FET device, characterized by the steps of:

providing a semiconductor substrate having a semiconductor layer (6) disposed over an insulator layer (4);

forming vertical semiconductor fins (12A) on top of the insulator layer (4) by etching parallel trenches (10A, 10B) through the semiconductor layer down to the insulator layer (4);

selectively depositing doped conductors (18A, 18B) at the bottoms of the trenches (10A, 10B) such that the doped source conductors contact bottom portions of the fins;

forming source insulators (20A, 20B) over the doped conductors (18A, 18B);

forming gate insulators (22) along sidewalls of the trenches;

thermally driving dopants from the doped conductors into bottom portions of the fins (12A) to form source regions (26A) in the fins (12A);

forming gate conductors (24A, 24B) along vertical sidewalls of the fins (12A), spaced away therefrom by the gate insulators (22);

doping top portions of the fins (12A) to form drain regions (28A) therein;

forming sidewall spacers (30) along exposed sidewalls of the trenches (10A, 10B), fins (12A) and gate conductors (24A, 24B);

etching back the source insulators to expose the underlying doped source conductors;

forming silicide in exposed portions of the source and gate conductors;

filling the trenches with an oxide trench-fill and planarizing; and

forming metal source, drain and gate contacts by Damascene processes of selective etching, metal fill, and chem-mech polishing.

21. A method of forming a vertical Fin-FET device according to claim 20 wherein the steps of forming source regions (26A) and drain regions (28A) effectively form channel regions in the fins (12A) extending between the source regions (26A) and drain regions (28A).

22. A method of forming a vertical Fin-FET device according to claim 20 wherein the semiconductor substrate is a silicon-on-insulator (SOI) substrate.